One Octave Bandwidth Rectifier With a Frequency Selective Diode Array

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***Abstract*— In this paper, a high-efficiency rectifier with one octave bandwidth is proposed by proposing a diode array with a frequency selective topology. With the frequency selective topology, the low-and high-band rectifiers are combined together without extra matching circuit at the input leading to a high-efficiency broadband design. For validation, a prototype rectifier was fabricated and characterized. The measured results show that the RF-dc power conversion efficiency (PCE) maintains above 70% from 1.75 to 3.55 GHz at an input power of 10 dBm. The measured PCE remains more than 50% within 1.4–3.7 GHz and the $|S_{11}|$ is lower than −10 dB from 1.7 to 3.6 GHz.**

***Index Terms*— Broadband RF rectifier, energy harvesting (EH), frequency selection, high efficiency, impedance matching, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) and energy harvesting (EH) are promising microwave/RF technologies that offer to extend the battery life of a device and allow applications where wired power is hard to access or unavailable. Recently, broadband EH is becoming popular where a broadband rectifier is needed [1]. Besides, a WPT system is normally integrated with other high-speed communication system, such as simultaneous wireless information and power transfer (SWIPT) [2], wireless sensor networks [3], and so on. Hence, it is expected to have a rectifier with both high conversion efficiency and wide bandwidth.

For a rectifier, maintaining high overall RF-dc power conversion efficiency (PCE) with a wide frequency band is challenging. To tackle this problem, broadband rectifiers have been proposed. In [4], a fractional bandwidth of 21.5% was realized by a second-order branch-line coupler where the efficiency is more than 70% over a frequency band from 2.08 to 2.58 GHz. In [5], a broadband rectifier is proposed by maximizing the quality factor of its matching circuits. It realizes a maximum efficiency of 81% with a fractional bandwidth of 18.5% (efficiency > 70%). The rectifier in [6] employs a nonuniform transmission line that can harvest RF energy in a frequency range from 400 MHz to 1 GHz for an efficiency that is more than 50%. A broadband rectifier in [7] is matched by three section stepped impedance transformers, the rectifying circuit demonstrates a 57% fractional bandwidth (1.65–3.05 GHz) with an efficiency that is higher than 50%. For efficiency of more than 70%, its bandwidth is reduced to 2%. A high-efficiency rectifier with extended operating bandwidth is presented in [8]. This structure shows more than 70% efficiency of about 45%. In [9], a two-level impedance match network was proposed at the input, the bandwidth of more than 70% efficiency is 40% (1.80–2.72 GHz).

In this paper, we propose a broadband rectifier with a frequency selective diode array for WPT or EH. Two diodes are integrated together with a frequency selective topology. With the frequency selective topology, complicated matching circuits are avoided which lead to a simplified circuit structure, a reduction in insertion loss, and a compact size. The fabricated rectifier shows one octave bandwidth (1.75–3.55 GHz) with PCE exceeding 70%.

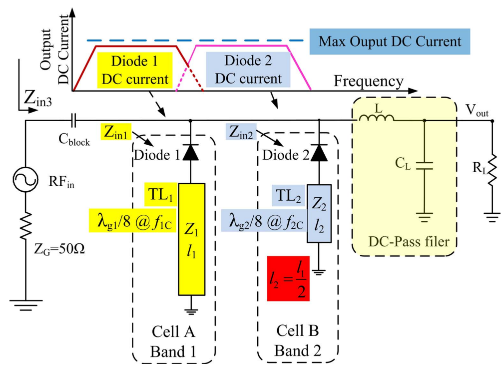

Fig. 1. Schematic of the proposed broadband rectifier with a frequency selective diode array.

II. Design and Simulation

Fig. 1 shows the block diagram of the proposed rectifier. It consists of a dc block capacitor C_{block}, a low band rectifier Cell A (Band 1), a high band rectifier Cell B (Band 2), and a dc-pass filter. The length of transmission line 2 (TL2) in Cell B is half of that of the TL1 in Cell A. An L-type low-pass filter is used to block the in-band input RF signal and its harmonics. The center frequency of the low band (Cell A) and that of the high band (Cell B) are denoted as f_{1c} and f_{2c}, respectively. The frequency ratio is $k = f_{1c}/f_{2c}$, and k is set to be 2.

As shown in Fig. 1, the rectifier in Cell A operating at the low band is matched at f_{1c} by a short circuit stub (TL1), which has a characteristic impedance of Z_1 and an electrical length of $\lambda_{g1}/8$ at f_{1c}. Cell B is the other rectifier operating at f_{2c} with another short circuit stub with a characteristic of Z_2 and an electrical length of $\lambda_{g2}/8$. Here, λ_{g1} and λ_{g2} are the guided wavelengths in the transmission lines at f_{1c} and f_{2c}, respectively. In Cell A, the input impedance of the eighth wavelength $\lambda_{g1}/8$ short circuit stub at different frequencies

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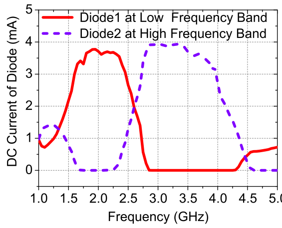

Fig. 2. Simulated dc currents of diodes 1 and 2 versus frequency.

(dc, f_{1c}, and f_{2c} ($f_{2c} = 2f_{1c}$) are described as follows [10]:

$$Z_{\lambda g1/8} = jZ_1 \tan\left(\frac{\pi}{4}\frac{f}{f_{1c}}\right) = \begin{cases} 0, & f = 0 \\ jZ_1, & f = f_{1c} \\ \infty, & f = 2f_{1c} = f_{2c}. \end{cases} \tag{1}$$

Equation (1) shows that the input impedance of Cell A is ∞ at f_{2c}, which implies that this branch is open in Band 2 centered at f_{2c}. In Cell B, the input impedance of TL2 at f_{1c} is $Z_{\lambda g2/8}(f_{1c}) = jZ_2\tan(\pi/4 * f/(2 * f_{1c})) \approx 0.4jZ_2$ that Cell B is switched OFF in Band 1 centered at f_{1c} due to impedance mismatch. Therefore, the structure is frequency selective which selects Cell A in Band 1 and Cell B in Band 2. Consequently, this leads to a broadband performance at the output. The insert at the top of Fig. 1 shows the output dc currents of the proposed rectifier versus frequency, which shows the broadband behavior caused by the frequency selection. The output dc current is contributed by either Diode 1 in Cell A or Diode 2 in Cell B depending on the frequency, $\mathrm{dc}_{\mathrm{out}}(f) = \mathrm{dc}_A(f) + \mathrm{dc}_B(f)$. As shown, Diode 1 is turned ON only in Band 1 whereas Diode 2 is turned ON only in Band 2, which shows the frequency selection in the proposed design and its broadband behavior. The frequency selection guarantees good isolation between the cells, leads to high conversion efficiency per rectifier cell and consequently better overall rectification efficiency across the whole band (Band 1 + Band 2).

The proposed circuit was simulated using the harmonic balance in Keysight Advance Design System. The simulated dc current of diodes versus frequency at 10-dBm input power is shown in Fig. 2. The rising and falling edges, overlap region of both dc currents can be clearly observed with the increase of frequency. In Fig. 2, the frequency selection on the operation of diodes can be clearly seen.

The matching of the rectifier Cells A and B is frequency selective. Based on (1), at the center frequency of the cell, the matching of an individual cell can be done by using the characteristic impedance of the short-ended TL to compensate the imaginary part of the input impedance looking into the cell and by adding a capacitor C_{add} to tune the real part when it is necessary. Details of matching are as follows.

Fig. 3 shows a detailed schematic of Cell A. As can be seen, for the diode at a given input power and dc load, the equivalent model can be denoted as R_e in parallel with a capacitor C_e. A small capacitor C_{add} in parallel with the diode is added for matching of the real part of the rectifier Cell A. Moreover, according to (1), the input impedance of the short stub (TL1) is jZ_1 at f_{1c}. Therefore, the input impedance Z_{in1} of Cell A can be described as follows:

$$Z_{\mathrm{in1}} = [(C_e + C_{\mathrm{add}}) \parallel R_e] + jZ_1. \tag{2}$$

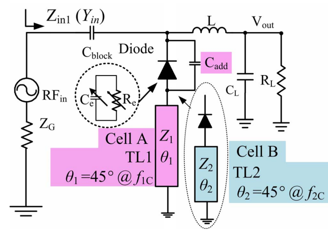

Fig. 3. Details of impedance matching for single cell.

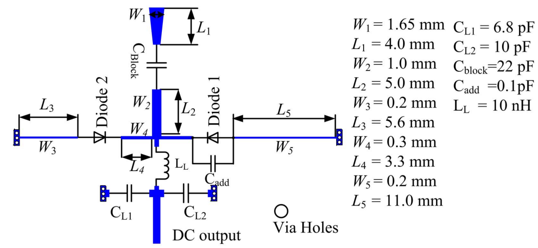

Fig. 4. Layout of the proposed rectifier.

Let $C_{\mathrm{sum}} = C_e + C_{\mathrm{add}}$, (2) can be rewritten as follows:

$$Z_{\mathrm{in1}} = \frac{R_e}{1 + (R_e\omega C_{\mathrm{sum}})^2} - j\frac{R_e^2\omega C_{\mathrm{sum}}}{1 + (R_e\omega C_{\mathrm{sum}})^2} + jZ_1. \tag{3}$$

For the real part of the input impedance Z_{in1} of Cell A, after a rearrangement, $\mathrm{Re}(Z_{\mathrm{in1}}) = 1/((1/R_e) + R_e(\omega C_{\mathrm{sum}})^2)$. As $(\omega C_{sum})^2$ is much smaller than 1, $\mathrm{Re}(Z_{\mathrm{in1}})$ can be reduced by increasing C_{sum} through a large C_{add}. On the other hand, based on (3), the imaginary part of Z_{in1} is set to be zero for matching by letting $Z_1 = R_e^2\omega C_{\mathrm{sum}}/(1 + (R_e\omega C_{\mathrm{sum}})^2)$. For Cell B, its corresponding working frequency is relatively high which corresponds to a low real part of the input impedance, adding C_{add} is not needed. Similarly, Z_2 can be determined by setting the imaginary part of the input impedance Z_{in2} of Cell B to be zero.

III. Implementation

The center frequencies, f_{1c} and f_{2c}, are set to be 1.8 and 3.6 GHz, respectively, for rectifying the RF energy from mobile phone station and Wi-Fi router (GSM 1800/1900 MHz and ISM 2.4 GHz). The proposed circuit was implemented and tested. The substrate used for this design is Rogers 4350B ($\epsilon_r = 3.66$ and $\tan\delta = 0.002$). The layout of the proposed broadband rectifier is shown in Fig. 4 with detailed dimensions. As can be seen, two HSMS-286B diodes with their short circuit stubs (TL1 and TL2) are connected to one single node directly. A chip capacitor $C_{\mathrm{add}} = 0.1$ pF was added in parallel with Diode 1 to adjust the real part of Z_{in1} at f_{1c}. The dc-pass filter is used to choke the in-band RF signal and the high order harmonics before the load R_L. Besides, the capacitor C_{block} (22 pF) was used for dc block and the load R_L is 400Ω.

IV. Experimental Results

Fig. 5 shows the schematic and a photograph of measuring setup. The RF signal generator (Anristu MG3692) was used to feed the proposed rectifier. By using a bidirectional coupler, the power sensor A measures the input power, and the spectrum analyzer measures the reflected fundamental and harmonic power at the input port. By varying the input power, frequency, the dc voltage was measured by digital meter

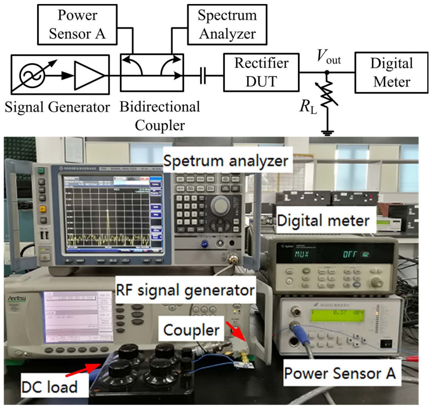

Fig. 5. Schematic and a photograph of the measuring setup.

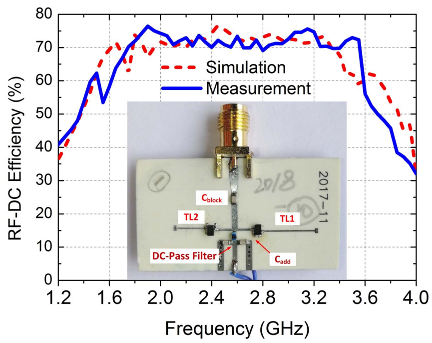

Fig. 6. Measured and simulated PCE versus frequency at 10 dBm.

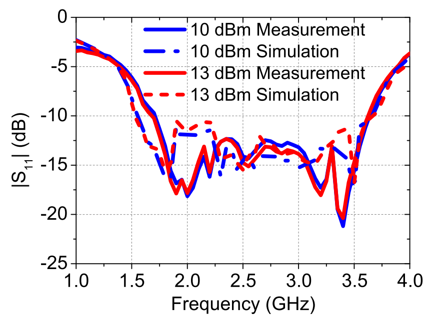

Fig. 7. $|S_{11}|$ versus frequency at 10- and 13-dBm input power.

(Agilent 34970) across the dc load R_L. The measured PCE is quantified as follows:

$$\eta_{\text{RF-dc}} = \frac{P_{dc}}{P_{\text{IN}}} \times 100\% = \frac{V_o^2}{R_L} \times \frac{1}{P_{\text{IN}}} \times 100\%. \quad (4)$$

The measured PCE versus frequency at 10 dBm is plotted in Fig. 6 together with the simulation results. Comparing the measurement and the simulation, they show good agreement. As shown, an efficiency of higher than 70% can be achieved from 1.75 to 3.55 GHz, which corresponds to a fractional bandwidth of 67.9%. Meanwhile, the measured efficiency is maintained at more than 50% from 1.4 to 3.7 GHz. The simulated and measured reflection coefficient $|S_{11}|$ at the input power of 10 and 13 dBm is shown in Fig. 7. The measured $|S_{11}|$ is better than -10 dB from 1.7 to 3.6 GHz, featuring one octave bandwidth and fractional bandwidth of 71.6%. The measured results agree with the simulated ones.

Table I shows a comparison of the performances between the proposed rectifier and the works featuring broadband in the literature. As shown, the proposed rectifier shows one octave bandwidth (67.9% fractional bandwidth) for efficiency higher than 70%, which is the highest among all the designs under comparison. Two diodes are used, and the physical size is 25×35 mm, which is the smallest among the four structures. The electrical size is as small as $0.2\lambda \times 0.28\lambda$.

TABLE I

COMPARISON WITH THE PRIOR RECTIFIERS

Reference	[5]	[8]	[9]	This work
BW for Efficency>70%	1.47-1.77	0.57-0.9	1.80-2.72	1.75-3.55
Fractional BW (Efficency>70%)	18.5%	44.9%	40%	67.9%
Input Power	10 dBm	12.8 dBm	19.5 dBm	10 dBm
Rectifier Element	HSMS286	HSMS286	HSMS282	HSMS286
Number of diode	2	1	1	2
Dimension(mm^2)	82×66	64×94	60×25	25×35
Electrical Size (λ^2)	0.38×0.1	0.15×0.2	0.45×0.18	0.2×0.28

⋆λ is the free-space wavelength at the center frequency of the operating band

V. CONCLUSION

A high-efficiency microwave rectifier using a diode array with an octave bandwidth was presented by proposing a frequency selection topology. In such a diode array, diodes working in two frequency bands are combined by using a frequency selection topology. With the proposed configuration, the complex matching circuit is avoided leading to a significant reduction of the insertion loss and a small circuit area. Consequently, the proposed topology maintains high-efficiency over a wide frequency range. For validation, a prototype operating at 1.4–3.7 GHz was fabricated and tested. The fractional bandwidth of efficiency higher than 70% is 67.9% (1.75–3.55 GHz). This proposed design method can be applied to the rectifier of other frequency band. Moreover, the proposed frequency selective topology can be applied to other circuit designs when frequency selection of different branches is needed.

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